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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/092,064	03/05/2002	Michael D. Scholten	AMCC-007XX	7833
207	7590	11/15/2005	EXAMINER	
WEINGARTEN, SCHURGIN, GAGNEBIN & LEOVICI LLP			NGUYEN, BINH QUOC	
TEN POST OFFICE SQUARE				
BOSTON, MA 02109			ART UNIT	PAPER NUMBER
			2664	

DATE MAILED: 11/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.



## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-6 are rejected under 35 U.S.C. 102(b) as being anticipated by *Osborne* the US Patent No: (US 6,078,733).

**Regarding claim 1;** *Osborne* teaches a link layer device including at least one unique identifier associated therewith, an input data line for receiving a plurality of received data packets, each of the plurality of data packets including a destination identifier and a plurality of data, the link layer device comprising:

a data receiver coupled to the input data line (*see Fig. 3, and Fig. 5, col. 12, lines 15-33, item 82 means a data receiver*);

a channel mapper coupled to the data receiver (*see Fig. 3, and Fig. 5, col. 12, lines 1-12, item 164 means a channel mapper*);

a received data FIFO coupled to the channel mapper (*see Fig. 3, and Fig. 5, col. 12, lines 11-12, item 160 means a received data FIFO*);

a feed-forward data FIFO coupled to the channel mapper (*see Fig. 3, and Fig. 5, col. 8, lines 29-47, "item DMA(Direct Memory Access) section 154" means a feed-forward data FIFO*); the channel mapper receiving the plurality of received data packets and being configured and arranged to divert the received data packets, having a destination identifier equivalent to the unique destination identifier, to the received data FIFO (*see col. 9, lines 10-29, and col. 11, lines 8-21*), and to divert the remaining plurality of received data packets to the feed-forward data FIFO (*see col. 11, line 22-to-col. 12, line 67*);

a transmitter data FIFO containing a plurality of data packets to be transmitted, each of the plurality of data packets to be transmitted having a destination identifier and a plurality of data (*see Fig. 3, and Fig. 9, col. 16, line 32-to-col. 17, line 59*); and

a data transmitter having an output coupled to an output data line, and an input coupled to the feed-forward data FIFO and to the transmitter data FIFO, the data transmitter configured and arranged to retrieve data packets from the feed-forward data FIFO and the transmitter data FIFO and to transmit the retrieved data packets on the output data line (*see Fig. 3, and Fig. 9, col. 16, lines 16-32*).

**Regarding claim 2.** *Osborne* teaches the link layer device of claim 1 further including an egress processor coupled to the received data FIFO and further coupled to a plurality of data ports, the egress processor configured and arranged to provide the received data packets contained in the received data FIFO to one of the plurality of data ports (*see Fig. 3, and Fig. 5, col. 12, lines 1-33, item processing buffer 158 means and egress processor*).

**Regarding claim 3.** *Osborne* teaches the system packet interface of claim 1 further including a data ingress processor coupled to the transmitter data FIFO and further coupled to a plurality of data ingress

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lines, the ingress processor configured and arranged to receive a plurality of data packets from the plurality of data ingress lines and to provide the received plurality of data packets as a plurality of data packets to be transmitted to the transmitter data FIFO (*see Fig. 3, and Fig. 9, col. 16, line 32-to-col. 17, line 10, item processing buffer 108 means a data ingress processor*).

**Regarding claim 4.** *Osborne* teaches the system packet interface of claim 1 wherein the output data line includes a plurality of output data lines (*see col. 8, lines 29-47 and col. 12, lines 1-16*).

**Regarding claim 5.** *Osborne* teaches the system packet interface of claim 1 wherein the input data line includes a plurality of input data lines (*see col. 8, lines 29-58*).

**Regarding claim 6.** *Osborne* teaches the system packet interface of claim 1 wherein the data transmitter is further coupled to a status line corresponding to the data output line and providing status indicia of a "data pass" "data no-pass" condition on the corresponding data output line (*see Fig. 3, and Fig. 9, col. 16, lines 16-31*), in the event the status indicia is "data no-pass" the data transmitter responsive to the status indicia by stopping transmission of data on the corresponding output data line, in the event the status indicia is "data pass" the data transmitter responsive to the status indicia by continuing transmission of data on the corresponding output data line (*see Fig. 3, and Fig. 9, col. 16, line 32-to-col. 17, line 59*).

### ***Allowable Subject Matter***

**Claims 7-10 are allowable.** The following is a statement of reasons for the indication of allowable subject matter: the prior art made of record fails to teach in combination of other limitations recited claims 7; A system for aggregating a plurality of input and output ports to a data

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device, the data device including a data output port and a data input port, the data device having a maximum data rate, the system comprising:

an egress processor coupled to the received data FIFO and further coupled to a data output port, the egress processor configured and arranged to provide the received data packets contained in the received data FIFO to the data output ports;

a data ingress processor coupled to the transmitter data FIFO and further coupled to a data input port, the ingress processor configured and arranged to receive a plurality of data packets from the data input port and to provide the received plurality of data packets, as a plurality of data packets to be transmitted, to the transmitter data FIFO;

the input data line of the first link layer device coupled to the output port of the data data device;

the output data line of the of the first link layer device being coupled to the input line of the second link layer device;

the output data line of the second link layer device being coupled to the input port of the data device;

wherein, the aggregate data rate of the first and second link layer devices is less than the maximum data rate of the data device.

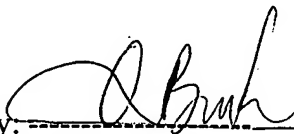
***Contact Information***

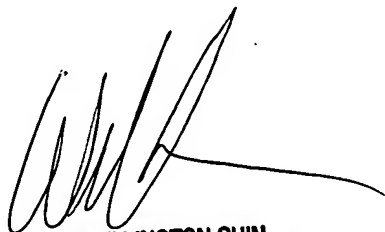
3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Binh Q. Nguyen whose telephone number is 571-272-8563. The examiner can normally be reached on M-F: 9:00 AM - 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wellington Chin can be reached on 571-272-3134. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Respectfully submitted,

By:   
Binh Q. Nguyen  
Patent Examiner  
11/11/2005

  
WELLINGTON CHIN  
SUPERVISORY PATENT EXAMINER